content of the key register, the content of the auxiliary memory being programmable only once.

8.(AMENDED) A circuit comprising a microprocessor (10) integrated with at least one first memory (2, 3), which includes a second auxiliary memory (20) adapted to containing at least one sub-program enabling authorizing the execution of a function of access to said first memory (2, 3), said auxiliary memory (20) being programmable only once.

9.(AMENDED) The circuit of claim 8, further including means (22) for selecting, at the input of a memory interface (14) of the microprocessor (10), a memory from among at least:

said auxiliary memory (20); and

said first memory (2, 3), the selection of said first memory, otherwise than for the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one also integrated storage element (2) and the content of the key register.

11.(AMENDED) The circuit of claim 8, further including means (24) for generating a priority-holding interrupt for executing said sub-program, the generation occurring provided that:

a signal (MODE) indicative of an access-control-operating mode is in an active state;

an access to the first memory (2) has been requested otherwise than for a non-interruptible execution of one of the functions that it contains; and

an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, the resulting priority-holding interrupt being non-interruptible, even by itself.

12.(AMENDED) The circuit of claim 8, further including means for implementing access to all or part of a content of the first memory (2, 3) integrated with the microprocessor, using a priority-holding interrupt (PRIORIN) and at least one register of keys (21), and applying at least one access control algorithm of at least one also integrated storage element (2) and the content of the key register, the content of the auxiliary memory being programmable only once.